REMARKS

These comments are responsive to the Official Action mailed on Office Action mailed on October 18, 2004. Claims 63-77 and 80-124 are currently pending. The Office Action rejected these claims for failure to comply with 37 CFR 1.607(a)(2-4), specifically, for not providing a proposed count, identifying at least one claim in each of the present application and an application with which an interference is sought, and explaining why any discrepancies between such claims and the proposed count.

In response, the following is proposed as a first count:

Count 1

For an electrically alterable non-volatile multi-level memory device including a plurality of non-volatile multi-level memory cells, each of the multi-level memory cells including a floating gate FET having a channel with electrically alterable voltage threshold value, the plurality of non-volatile multi-level memory cells being disposed in a matrix of rows and columns, channels of multi-level memory cells of a first group of the plurality of non-volatile multi-level memory cells being coupled in parallel between a first bit line and a reference potential, channels of multi-level memory cells of a second group of the plurality of non-volatile multi-level memory cells being coupled in parallel between a second bit line and the reference potential, electrons being capable of being injected into the floating gate from the channel of each of the plurality of non-volatile multi-level memory cell, electric currents flowing through the channels of the multi-level memory cells of the first group and electric currents flowing through the channels of the multi-level memory cells of the second group being substantially flowing in a same direction, a method of operating the electrically alterable non-volatile multi-level memory device, comprising:

settling a parameter of at least one non-volatile multi-level memory cell of the plurality of non-volatile multi-level memory cells to one state selected from a plurality of states including at least a first state, a second state, a third state and a fourth state in response to information to be stored in the one non-volatile multi-level memory cell,

verifying whether the parameter of the one non-volatile multi-level memory cell has being settled to the one state selected from the plurality of states by comparing the parameter of the one non-volatile multi-level memory cell with a plurality of verifying reference parameters including at least a first verifying reference parameter, a second verifying reference parameter, a third verifying reference parameter and a fourth verifying reference parameter, and of repeating the operation for settling the parameter and the operation for verifying until it is verified by the operation for verifying that the parameter of the one non-volatile multi-level memory cell has being settled to the one state,

reading status of the one non-volatile multi-level memory cell by comparing the parameter with a plurality of reading reference parameters including at least a first reading reference parameter, a second reading reference parameter and a third reading reference parameter,

wherein a conductivity value of the one non-volatile multi-level memory cell is decreased in order of the first state, the second state, the third state and the fourth state,

wherein the first reading reference parameter is allocated between the first state and the second state, the second reading reference parameter is allocated between the second state and the third state, and the third reading reference parameter is allocated between the third state and the fourth state,

wherein the first reading reference parameter, the second reading reference parameter and the third reading reference parameter are parameters for a normal read operation in which the information stored in the one non-volatile multi-level memory cell can be read out by output data of a plurality of bits,

wherein the normal read operation is carried out by parallel-comparing the parameter with the plurality of reading reference parameters by using a plurality of sense circuits including at least a first sense circuit, a second sense circuit and a third sense circuit, first input terminals of the first sense circuit, the second sense circuit and the third sense circuit are commonly supplied with the parameter from the one non-volatile multi-level memory cell, a second input terminal of the first sense circuit is supplied with the first reading reference parameter, a second input terminal of the second sense circuit is supplied with the second reading reference parameter and a second input terminal of the third sense circuit is supplied with the third reading reference parameter, and

wherein the first verifying reference parameter is allocated below the first reading reference parameter, the second verifying reference parameter is allocated between the first reading reference parameter and the second reading reference parameter, the third verifying reference parameter is allocated between the second reading reference parameter and the third reading reference parameter and the fourth verifying reference parameter is allocated above the third reading reference parameter.

The proposed Count 1 corresponds to, and is the same as, claim 63 of the present application; it also corresponds to claim 1 of U.S. patent 6,014,327 and differs from claim 1 (and claim 7) of U.S. patent 6,014,327 only in that it does not specify the specific mechanism of electron injection.

The proposed Count 1 may be taken to also corresponds to claim 1 of U.S. patent 6,356,486 and differs from claim 1 (and claim 7) of U.S. patent 6,356,486 in that it does not specify the specific mechanism of electron injection and recites certain structural detail differently. (Alternately, claim 80 of the present application could be used as an alternate or additional count, as it differs from claim 1 (and claim 7) of U.S. patent 6,356,486 only in that it does not specify the specific mechanism of electron injection.)

The proposed Count 1 may be taken to also corresponds to claim 1 of U.S. patent 6,381,172 and differs from claim 1 of U.S. patent 6,381,172 in that it is a device claim rather than a method claim and recites the various limitations somewhat differently. (Alternately,

claim 94 of the present application could be used as an alternate or additional count, as it is a copy of claim 1 of U.S. patent 6,381,172.)

The proposed Count 1 may be taken to also corresponds to claim 1 of U.S. patent 6,404,675 and differs from claim 1 of U.S. patent 6,404,675 in that it is a device claim rather than a method claim and recites the various limitations somewhat differently. (Alternately, claim 107 of the present application could be used as an alternate or additional count, as it is a copy of claim 1 of U.S. patent 6,404,675.)

Reconsideration of the rejections of claims 63-77 and 80-124 and an early indication of their allowance are solicited, and if there are any questions about the proposed Count or other matters related to this case, a call to the undersigned is invited.

Respectfully submitted,

Gerald P. Parsons — Date: Jan. 14, 2005

Gerald P. Parsons
Reg. No. 24,486

PARSONS HSUE & DE RUNTZ LLP
655 Montgomery Street, Suite 1800
San Francisco, CA 94111
(415) 318-1160 (main)
(415) 318-1163 (direct)
(415) 693-0194 (fax)